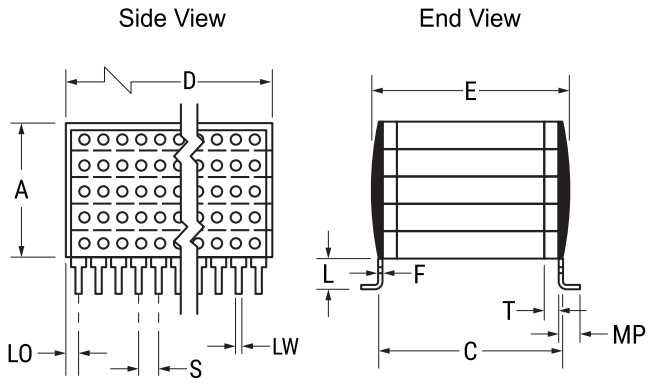
T49470X01825KBL

Aliases (L1XL401825KT65)

KPS LDD Mil SMPS PRF49470, Ceramic, 8.2 uF, 10%, 100 VDC, BX, N/A



Click here for the 3D model.

General Information	
Series	KPS LDD Mil SMPS PRF49470
Style	Leaded Stacked Chip
Description	Low ESR, High Current Stacked Ceramic Chips
Features	Low ESR, High Current
RoHS	No
Prop 65	**WARNING:** Cancer and reproductive harm - https://www.p65warnings.ca.gov./
SCIP Number	1397a5ac-1739-4afc-b57f-5edc4c8a9f53
Termination	60/40 Solder Coated
Lead	L Leads
Failure Rate	N/A
Testing and Reliability	Level T
Qualifications	MIL-PRF-49470
Notes	Note: Number of chips in stack depends on design. Note: Turn Radius For Lead Extension Is 0.1 Radians (Typical). Note: Lead alignment within pin rows shall be within ±.0.13 mm.

Dimensions	
D	9.845mm +/-0.955mm
L	1.78mm +/-0.25mm
T	1.397mm MAX
S	2.54mm TYP
F	0.254mm +/-0.051mm
A	16.51mm MAX
C	10.16mm +/-0.635mm
E	11.18mm MAX
LO	1.586mm MAX
LW	0.508mm +/-0.051mm
MP	1.27mm MIN

Specifications	
Capacitance	8.2 uF
Tolerance	10%
Voltage DC	100 VDC
Dielectric Withstanding Voltage	250 VDC
Temperature Range	-55/+125°C
Temp. Coefficient	BX
Dissipation Factor	2.5%
Insulation Resistance	121.951 MOhms

Packaging Specifications	
Packaging	Waffle, Box
Packaging Quantity	36

Statements of suitability for certain applications are based on our knowledge of typical operating conditions for such applications, but are not intended to constitute - and we specifically disclaim - any warranty concerning suitability for a specific customer application or use. This Information is intended for use only by customers who have the requisite experience and capability to determine the correct products for their application. Any technical advice inferred from this Information or otherwise provided by us with reference to the use of our products is given gratis, and we assume no obligation or liability for the advice given or results obtained.

© 2006 - 2026 YAGEO