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**General Information**

Series	KPS LDD Mil SMPS PRF49470
Style	Leaded Stacked Chip
Description	Low ESR, High Current Stacked Ceramic Chips
Features	Low ESR, High Current
RoHS	No
Prop 65	<b>WARNING:</b> Cancer and reproductive harm - <a href="https://www.p65warnings.ca.gov/">https://www.p65warnings.ca.gov/</a>
SCIP Number	1397a5ac-1739-4afc-b57f-5edc4c8a9f53
Termination	60/40 Solder Coated
Lead	Wire Leads
Failure Rate	N/A
Testing and Reliability	Level T
Qualifications	MIL-PRF-49470
Notes	Note: Number of chips in stack depends on design. Note: Lead alignment within pin rows shall be within ±0.13 mm.

**Dimensions**

D	9.845mm +/-0.955mm
L	6.35mm MIN
T	1.397mm MAX
S	2.54mm TYP
F	0.254mm +/-0.051mm
A	9.144mm MAX
C	10.16mm +/-0.635mm
E	11.18mm MAX
G	1.4mm +/-0.254mm
LO	1.586mm MAX
LW	0.508mm +/-0.051mm

**Packaging Specifications**

Packaging	Waffle, Box
Packaging Quantity	36

**Specifications**

Capacitance	2.2 uF
Tolerance	10%
Voltage DC	200 VDC
Dielectric Withstanding Voltage	500 VDC
Temperature Range	-55/+125°C
Temp. Coefficient	BR
Dissipation Factor	2.5%
Insulation Resistance	454.545 MOhms

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