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General Information

Series	KPS LDD Mil SMPS PRF49470
Style	Leaded Stacked Chip
Description	Low ESR, High Current Stacked Ceramic Chips
Features	Low ESR, High Current
RoHS	No
Prop 65	WARNING: Cancer and reproductive harm - https://www.p65warnings.ca.gov/
Termination	60/40 Solder Coated
Lead	J Leads
Failure Rate	N/A
Testing and Reliability	Level B
Qualifications	MIL-PRF-49470
Notes	Note: Number of chips in stack depends on design. Note: Turn Radius For Lead Extension Is 0.1 Radians (Typical). Note: Lead alignment within pin rows shall be within ±0.13 mm.

Dimensions

D	6.335mm +/-0.645mm
L	1.78mm +/-0.25mm
T	1.397mm MAX
S	2.54mm TYP
F	0.254mm +/-0.051mm
A	3.048mm MAX
C	6.35mm +/-0.635mm
E	7.62mm MAX
LO	1.586mm MAX
LW	0.508mm +/-0.051mm
MP	1.27mm MIN

Specifications

Capacitance	0.68 uF
Tolerance	20%
Voltage DC	100 VDC
Dielectric Withstanding Voltage	250 VDC
Temperature Range	-55/+125°C
Temp. Coefficient	BX
Dissipation Factor	2.5%
Insulation Resistance	1.4706 GOhms

Packaging Specifications

Packaging	Waffle, Box
Packaging Quantity	64

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