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### General Information

Series	KPS LDD Mil SMPS PRF49470
Style	Leaded Stacked Chip
Description	Low ESR, High Current Stacked Ceramic Chips
Features	Low ESR, High Current
RoHS	No
Prop 65	<b>WARNING:</b> Cancer and reproductive harm - <a href="https://www.p65warnings.ca.gov/">https://www.p65warnings.ca.gov/</a>
SCIP Number	2499890a-0e07-42ff-98a1-bd02d3b7c2ec
Termination	60/40 Solder Coated
Lead	Wire Leads
Failure Rate	N/A
Testing and Reliability	Level B
Qualifications	MIL-PRF-49470
Notes	Note: Number of chips in stack depends on design. Note: Lead alignment within pin rows shall be within $\pm 0.13$ mm.

Dimensions	
D	6.335mm +/-0.645mm
L	6.35mm MIN
T	1.397mm MAX
S	2.54mm TYP
F	0.254mm +/-0.051mm
A	6.096mm MAX
C	6.35mm +/-0.635mm
E	7.62mm MAX
G	1.4mm +/-0.25mm
LO	1.586mm MAX
LW	0.508mm +/-0.051mm

Specifications	
Capacitance	2.2 uF
Tolerance	10%
Voltage DC	50 VDC
Dielectric Withstanding Voltage	125 VDC
Temperature Range	-55/+125°C
Temp. Coefficient	BX
Dissipation Factor	2.5%
Insulation Resistance	454.545 MOhms

Packaging Specifications	
Packaging	Waffle, Box
Packaging Quantity	64

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