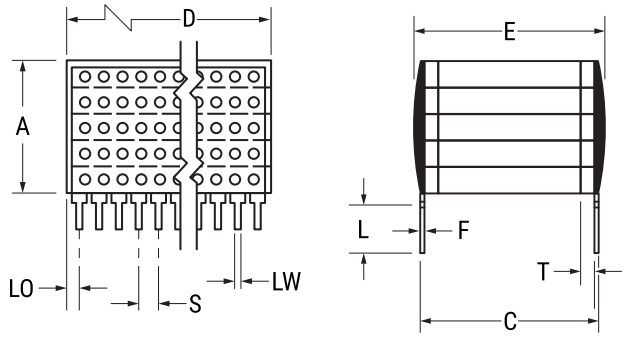
M49470Q01565MEN

Aliases (L1QN30C565MB65)

KPS LDD Mil SMPS PRF49470, Ceramic, 5.6 uF, 20%, 500 VDC, BQ, N/A

Side View

End View



Click here for the 3D model.

General Information	
Series	KPS LDD Mil SMPS PRF49470
Style	Leaded Stacked Chip
Description	Low ESR, High Current Stacked Ceramic Chips
Features	Low ESR, High Current
RoHS	No
Prop 65	**WARNING:** Cancer and reproductive harm - https://www.p65warnings.ca.gov./
SCIP Number	2499890a-0e07-42ff-98a1-bd02d3b7c2ec
Termination	60/40 Solder Coated
Lead	Wire Leads
Failure Rate	N/A
Testing and Reliability	Level B
Qualifications	MIL-PRF-49470
Notes	Note: Number of chips in stack depends on design. Note: Lead alignment within pin rows shall be within ±.0.13 mm.

Dimensions	
D	25.715mm +/-1.585mm
L	6.35mm MIN
T	1.397mm MAX
S	2.54mm TYP
F	0.254mm +/-0.051mm
A	16.51mm MAX
C	11.43mm +/-0.635mm
E	12.7mm MAX
G	1.4mm +/-0.25mm
LO	1.586mm MAX
LW	0.508mm +/-0.051mm

Specifications	
Capacitance	5.6 uF
Tolerance	20%
Voltage DC	500 VDC
Dielectric Withstanding Voltage	750 VDC
Temperature Range	-55/+125°C
Temp. Coefficient	BQ
Dissipation Factor	2.5%
Insulation Resistance	178.571 MOhms

Packaging Specifications	
Packaging	Waffle, Box
Packaging Quantity	28

Statements of suitability for certain applications are based on our knowledge of typical operating conditions for such applications, but are not intended to constitute - and we specifically disclaim - any warranty concerning suitability for a specific customer application or use. This Information is intended for use only by customers who have the requisite experience and capability to determine the correct products for their application. Any technical advice inferred from this Information or otherwise provided by us with reference to the use of our products is given gratis, and we assume no obligation or liability for the advice given or results obtained.

© 2006 - 2026 YAGEO