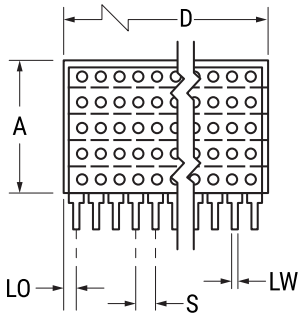
L1XN301276KC65

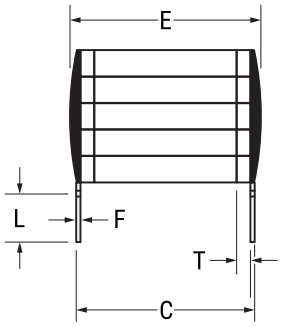
Aliases (87106091)

KPS LDD Comm SMPS, Ceramic, 27 uF, 10%, 100 VDC, BX, N/A

Side View



End View



Click here for the 3D model.

General Information	
Series	KPS LDD Comm SMPS
Style	Leaded Stacked Chip
Description	Low ESR, High Current Stacked Ceramic Chips
Features	Low ESR, High Current
RoHS	No
Prop 65	**WARNING:** Cancer and reproductive harm - https://www.p65warnings.ca.gov./
SCIP Number	df2a2509-5a11-4b26-944d-42278323ecf4
Termination	60/40 Solder Coated
Lead	Wire Leads
Failure Rate	N/A
Testing and Reliability	DSCC87106
Notes	Note: Number of chips in stack depends on design. Number of Chips in this stack = 5. Note: Lead alignment within pin rows shall be within ±.0.13 mm.

Dimensions	
D	25.715mm +/-1.585mm
L	6.35mm MIN
T	1.397mm MAX
S	2.54mm TYP
F	0.254mm +/-0.051mm
A	16.51mm MAX
C	11.43mm +/-0.635mm
E	12.7mm NOM
G	1.4mm +/-0.25mm
LO	1.586mm MAX
LW	0.508mm +/-0.051mm

Specifications	
Capacitance	27 uF
Tolerance	10%
Voltage DC	100 VDC
Dielectric Withstanding Voltage	250 VDC
Temperature Range	-55/+125°C
Temp. Coefficient	BX
Dissipation Factor	2.5% 1 kHz 25C
Aging Rate	1% Loss/Decade Hour
Insulation Resistance	3.7 GOhms

Packaging Specifications	
Packaging	Waffle, Box
Packaging Quantity	28

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